AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 2, lines 15-20 with the following paragraph, marked up to show changes made.

Another embodiment of the invention pertains to a method for targeted fault-tolerant computing in a central processing unit (CPU). The method includes decoding a fault-tolerant version of an instruction to generate a first op code and decoding a non-fault-tolerant version of the instruction to generate a second op code. The first op code is executed with redundancy checking. The second op code [[Is]] is executed without redundancy checking.